REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

Claims 1-20 are pending in this patent application.

In the present Office Action dated September 20, 2006, the Examiner rejected Claims 1, 12, 16 and 20 were rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Maley et al. (US 5,915,107) ("Maley"). The Examiner did indicate that Claims 2-11, 13-15 and 17-19 presented allowable subject matter for which the Examiner is respectfully thanked.

With respect to the rejection of each independent Claims 1, 12, 16 and 20, Applicants respectfully disagree.

The present invention as claimed in Claim 1, includes the recitation that a first clock signal operates in a first clock domain and a second clock signal operates in a second clock domain, said first and second clock signals of the same frequency but operating out of phase. In the office action, the Examiner appears to liken signals PLCK and BLCK as the respective first and second clock signal of the present invention. However, the relationship between these signals is not the same as the relationship between the first clock signal (operating in a first clock domain) and a second clock signal (operating in a second clock domain) as claimed. That is, Maley teaches that the PCLK and BCLK are not the same frequency as each other. For instance, in the passage in Maley at col. 4, lines 25-32, it is indicated how the frequency of the PCLK signal (a processor clock signal) is a half-integer (N/2) multiple of the frequency of the BCLK signal (a bus clock signal). This, respectfully, does not anticipate the teaching of the present invention as claimed that requires the first clock signal (operating in a first clock domain) and a second clock signal (operating in a second clock domain) to be of the same frequency but out of phase. Thus, Maley is attempting to solve another problem of

handling transfers from bus domain circuit to a processor core domain circuit. The present invention, on the other hand, is concerned with data transmit circuit and receive circuits that meet the clocking criteria as set forth in the claims -that the first clock and second clock are of the same frequency and out of phase.

Further in the rejection, the Examiner likens the claimed buffer circuit as comprising the latch means 135 as shown in Fig. 1B and Fig. 2. While not suggesting at all that this latch circuit functions similarly as the buffer circuit as claimed in claim 1, at a minimum, the analysis should determine the correct functionality of this latch circuit for the situation where the frequency of the first and second clock domains are the same, e.g., as Claim 1 requires. As it turns out, this situation happens to be addressed at col. 6, lines 65- col. 7, line 1 of Maley. That is, when "N" is even, e.g., N=2, there are N/2 cycles of signal PCLK per cycle of signal BCLK, and "each rising edge of bus clock signal BCLK is approximately synchronized with a rising edge of signal PCLK". This is actually reinforced in the discussion of Fig. 2 that, when PCLK frequency is an integer multiple of frequency of BCLK the CLKENH is always deasserted and only the CLKENL is asserted. Further, Maley teaches at col. 5, lines 15-17 that the assertion of CLKENL signal enables latching of the signal on the rising edge of signal PCLK. The obvious conclusion is that for the case where the f_B (BCKLK) and f_P (PCLK) frequencies are the same, the signals crossing between the clock domain of the processing core and the clock domain of the system bus enter the storage element that has a valid output value at a rising edge of the processor clock signal only (because CLKENH is always deasserted for this case).

Thus, Maley does not really teach a solution for the situation being solved by the present invention, i.e., the handling of signals crossing between the clock domain of a transmit processing core and receive processing core wherein the clock signals in each

domain are at the same frequency but operating out of phase. Thus, respectfully, applicants fail to see how the Maley's latch means 135 is teaching of the claimed buffer (comprising data path 200 including latches 200, 220, 230 as in Fig. 2 of the present application).

Moreover, notwithstanding the cited passage in Maley in Claim 1 directed to control logic that during each cycle of the first clock signal, "generates a control signal indicating whether a rising edge or a falling edge of the second clock signal is closest to being synchronized with a selected edge of the first clock signal" –again, this is really directed to the main solution of enabling latching of signals crossing between the two clock domains wherein the clock signals in the second domain (processor) are at "non-integer multiples" of the clock signals in the first domain (bus).

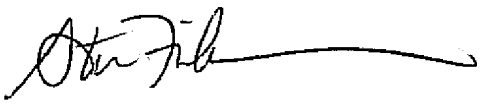
For these reasons, the cited Maley reference cannot be said to be anticipatory as each of the limitations of the claim have not been met. Moreover, even assuming that Maley addresses the situation of identical clock frequencies in each of the signal crossing clock domains, it does not address the out of phase relationship between these clock signals when crossing circuits of differing clock domains as addressed in the present invention. That is, by virtue of provision of PLL 195 as shown in Figure 1D of Maley, no out of phase issues exist. That is, as shown in Maley's Figure 1D, the first clock domain signal PCLK will always be a half-integer multiple of the second clock domain signal frequency BCLK. This provision thus obviating the need to make a phase relationship determination in Maley.

As Claim 20 was originally silent to this out of phase relationship, the preamble of Claim 20 is being amended to correspond to the preambles of the other independent claims 1, 12 and 16, that is, to set forth the first and second clock signals of the same frequency but operating out of phase at the differing clock domains.

In view of the amendments provided herein to the Claims 20, and, in view of the Remarks herein, applicants respectfully request that the Examiner withdraw all rejections of independent Claims 1, 12 and 16 and withdraw the rejection of amended Claim 23 and to withdraw the rejections of all remaining claims dependent thereon.

In view of the foregoing remarks herein, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with the Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned, Applicants' attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,



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